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Title: SIDE TABLES ANNOTATING AN INSTRUCTION STREAM

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Examiner: David Eng

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Exhibit 1	Clean version of the entire set of pending claims (37 C.F.R. 1.121(c)(3))
Exhibit 2	Rewritten claims marked up to show changes (37 C.F.R. 1.121(c)((1)(ii))
Exhibit 3	Excerpts from ANDREW S. TANENBAUM, STRUCTURED COMPUTER ORGANIZATION, 2d ed., Prentice-Hall (1984)
Exhibit 4	Excerpts from John Hennessy and David Patterson, Computer Architecture: A Quantitative Approach, William Kaufman Pub., San Mateo CA (1990)
Exhibit 5	Excerpts from INTEL CORP., INTEL ARCHITECTURE SOFTWARE DEVELOPER’S MANUAL, vol. 1 (1997)
Exhibit 6	Excerpts from Intel Corp., Intel Architecture Software Developer’s Manual, vol. 2 (1997)
Exhibit 7	Excerpts from INTEL CORP., INTEL ARCHITECTURE SOFTWARE DEVELOPER’S MANUAL, vol. 3 (1997)
Exhibit 8	Instruction Set Architecture Testing, from www.informatik.uni-bremen.de/~davinci/applications/dgm_paper.ps ; Guest Viewpoint: Is Out-of-Order Out of Date? Microprocessor Report (Feb 7, 2000) from www.hp.com/products1/itanium/infolibrary/reports/hp_ia64.pdf ; and Patterson & Yelick, Bridging the Processor-Memory Gap, www.ucop.edu/research/micro/99_00/99_094.pdf

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